Embedded Processor-Based Self-Test (Frontiers in Electronic Testing)

Dimitris Gizopoulos, A. Paschalis, Yervant Zorian

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Embedded Processor-Based Self-Test is a guide to self-testing strategies for embedded processors. Embedded processors are regularly used today in most System-on-Chips (SoCs). Testing of microprocessors and embedded processors has always been a challenge because most traditional testing techniques fail when applied to them. This is due to the complex sequential structure of processor architectures, which consists of high performance datapath units and sophisticated control logic for performance optimization. Structured Design-for-Testability (DfT) and hardware-based self-testing techniques, which usually have a non-trivial impact on a circuit's performance, size and power, can not be applied without serious consideration and careful incorporation into the processor design.

Embedded Processor-Based Self-Test shows how the powerful embedded functionality that processors offer can be utilized as a self-testing resource. Through a discussion of different strategies the book emphasizes on the emerging area of Software-Based Self-Testing (SBST). SBST is based on the idea of execution of embedded software programs to perform self-testing of the processor itself and its surrounding blocks in the SoC. SBST is a low-cost strategy in terms of overhead (area, speed, power), development effort and test application cost, as it is applied using low-cost, low-speed test equipment.

Embedded Processor-Based Self-Test can be used by designers, DfT engineers, test practitioners, researchers and students working on digital testing, and in particular processor and SoC test. This book sets the framework for comparisons among different SBST methodologies by discussing key requirements. It presents successful applications of SBST to a number of embedded processors of different complexities and instruction set architectures.

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