



Hybrid Spintronic/CMOS circuit design and analyse: Conception, Evaluation, Simulation and Implementation of hybrid Spintronic/CMOS circuits

Weisheng ZHAO, Eric BELHAIRE, Claude CHAPPERT

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In the past 20 years, programmable logic circuits have been rapidly developed. However, the intrinsic constraints such as data volatility and high leakage currents of CMOS technology cause more and more limits, such as data loss in case of power failures, the long latency to initialize the system and high standby power etc. This last point has become a major challenge for the minimization of the transistors sub 90nm. Recently, numerous emerging technologies have been proposed and explored to overcome these problems. Among them, spintronic technologies promise the most efficiency and potentials. This book focuses on the study, design, simulation and implementation of hybrid circuits combining CMOS technologies and non-volatile spintronic devices. The Magnetic Tunnel Junction (JTM) has been particularly studied. Hybrid circuits were first designed and simulated electrically. They show great potential in terms of speed, non-volatility and consumption compared to conventional circuits. They also enable new computing architectures and advanced modes of reconfiguration. Finally, a prototype was developed to demonstrate physically the behavior and performance of these circuits.

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